

FIG. 1

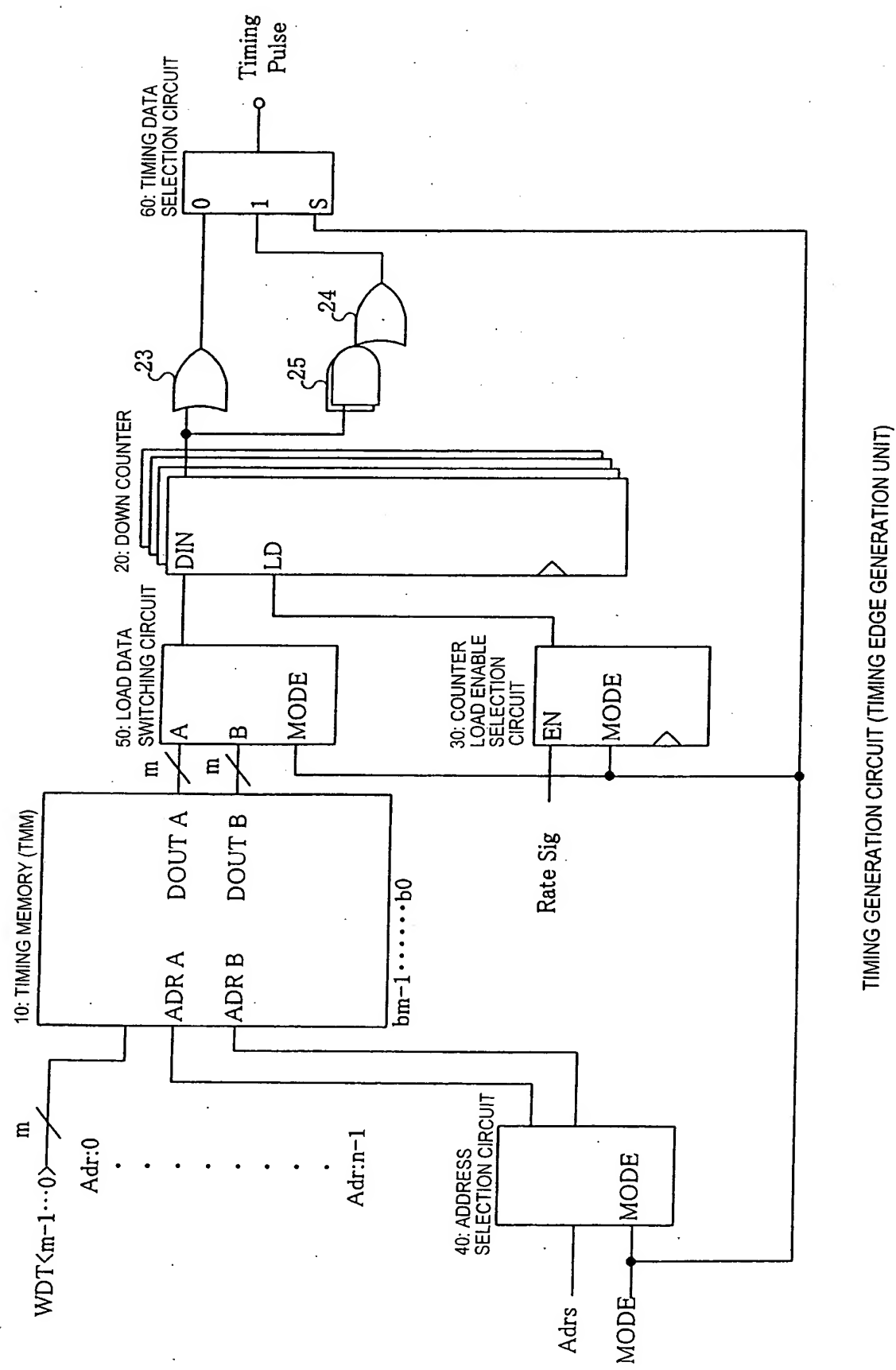


FIG. 2

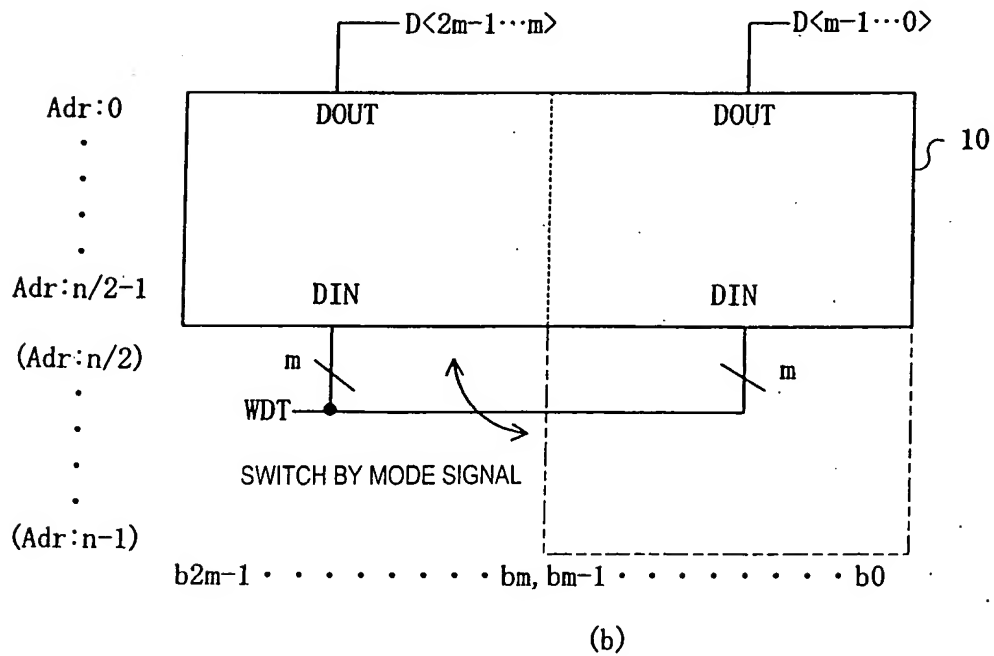
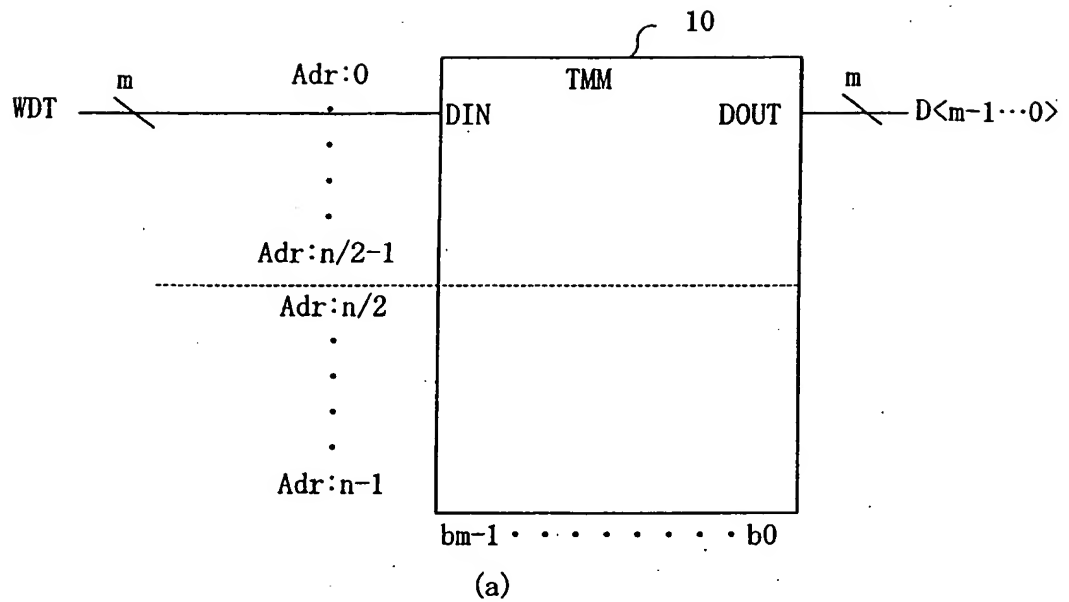


FIG. 3

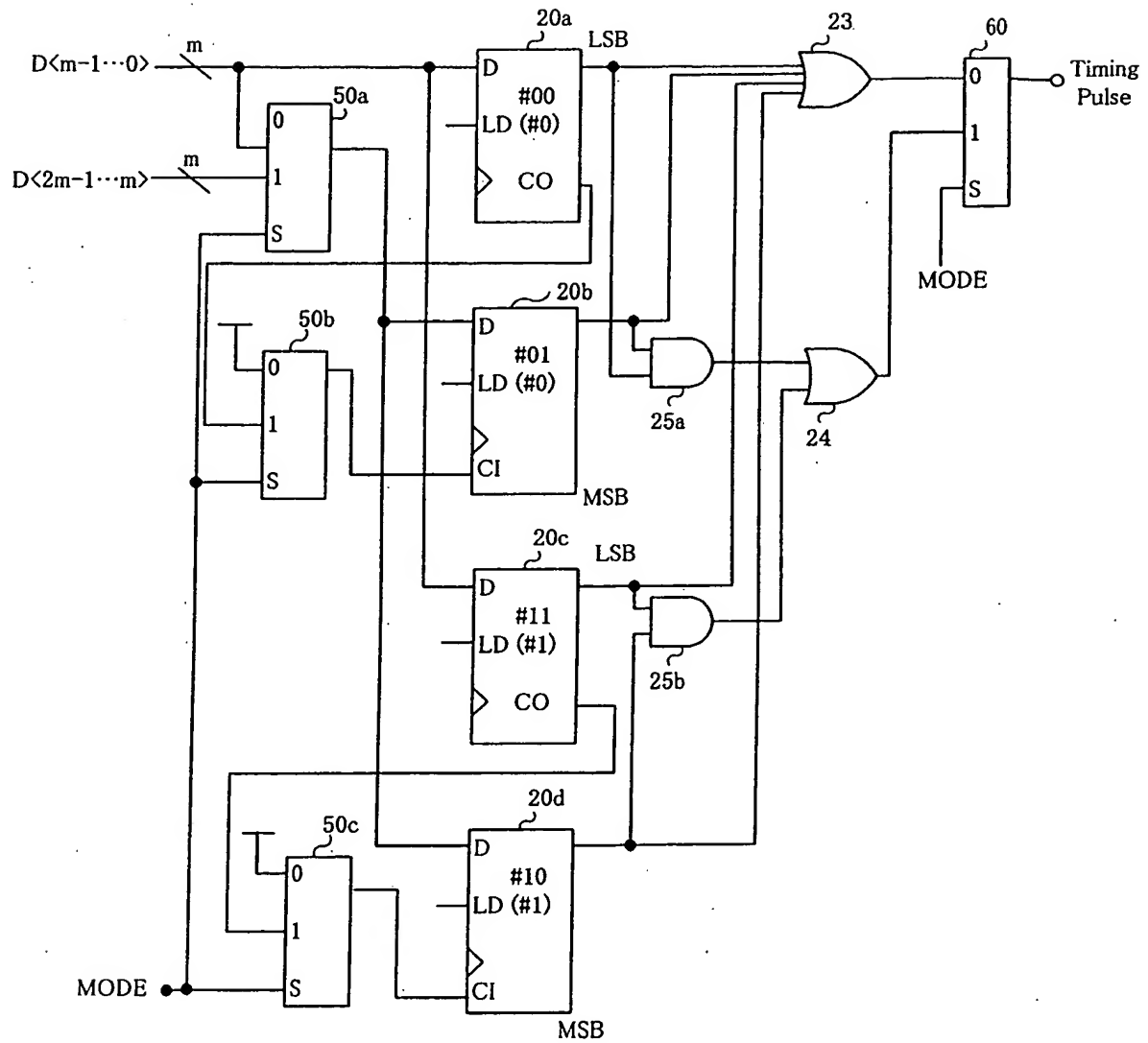
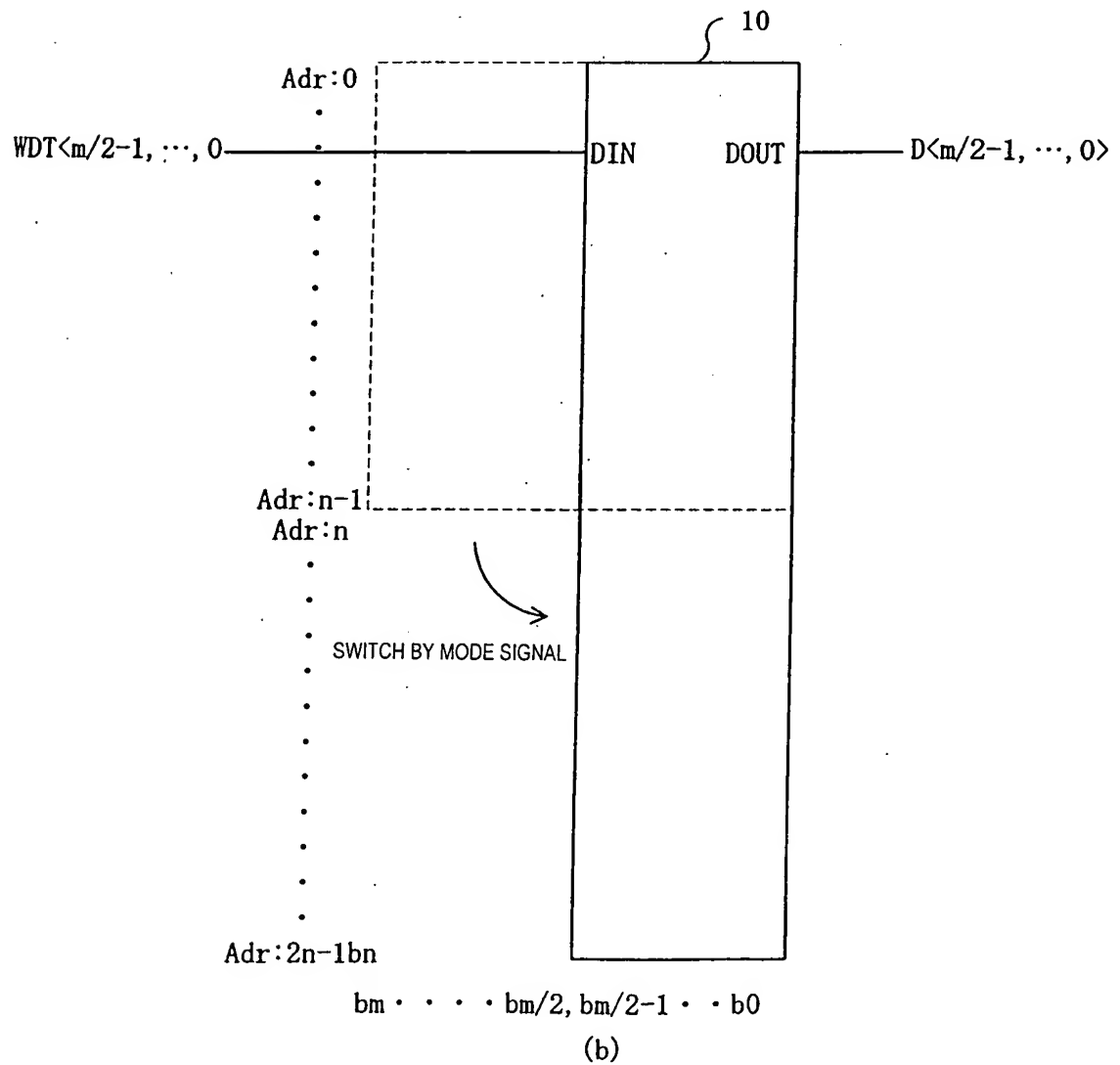
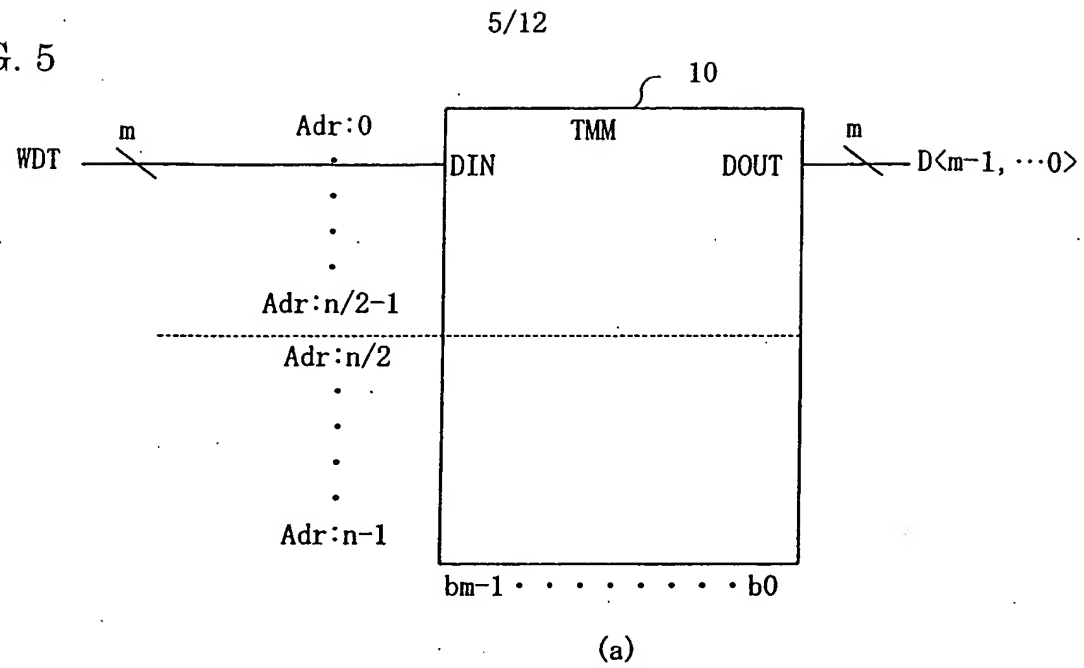


FIG. 4

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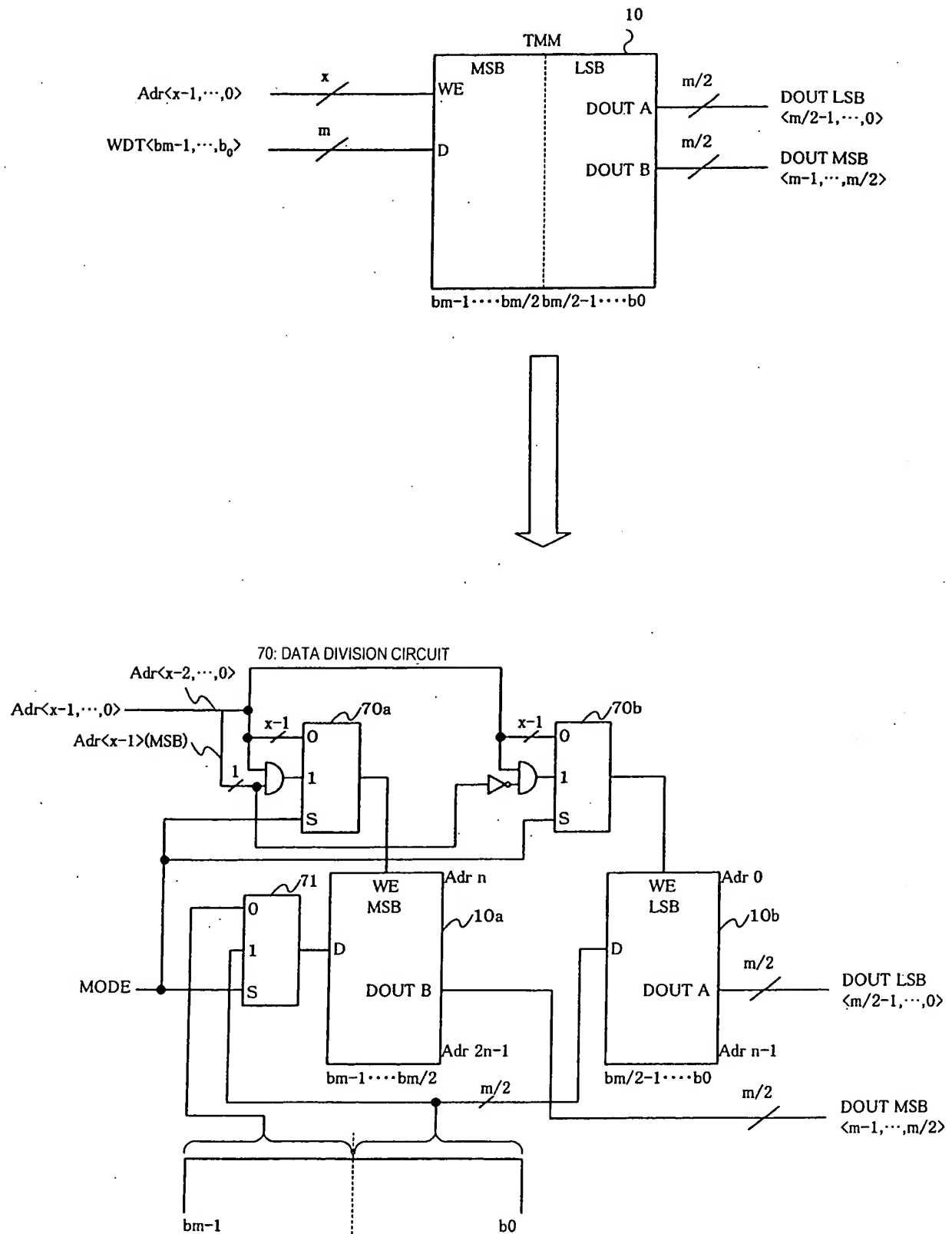
TMM				DOWN COUNTER		
STANDARD DELAY $T_G$ (mode=0)	TOTAL LATCH NUMBER	SET DATA BIT WIDTH	MEMORY DEPTH (TS NUMBER)	PHASE NUMBER	BIT NUMBER /PHASE	MAXIMUM TIMING DELAY
	$n \times m$	$m$	$n$	4	$m$	$\text{SysCLK}(2^{m-1}), m-1 \dots m$
LONG DELAY $T_G$ (mode=1)	$n/2 \times 2m$	$2m$	$n/2$	2	$2m$	$\text{SysCLK}(2^{M-1}), 1 \leq M \leq 2m$

FIG. 5



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FIG. 6



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FIG. 7

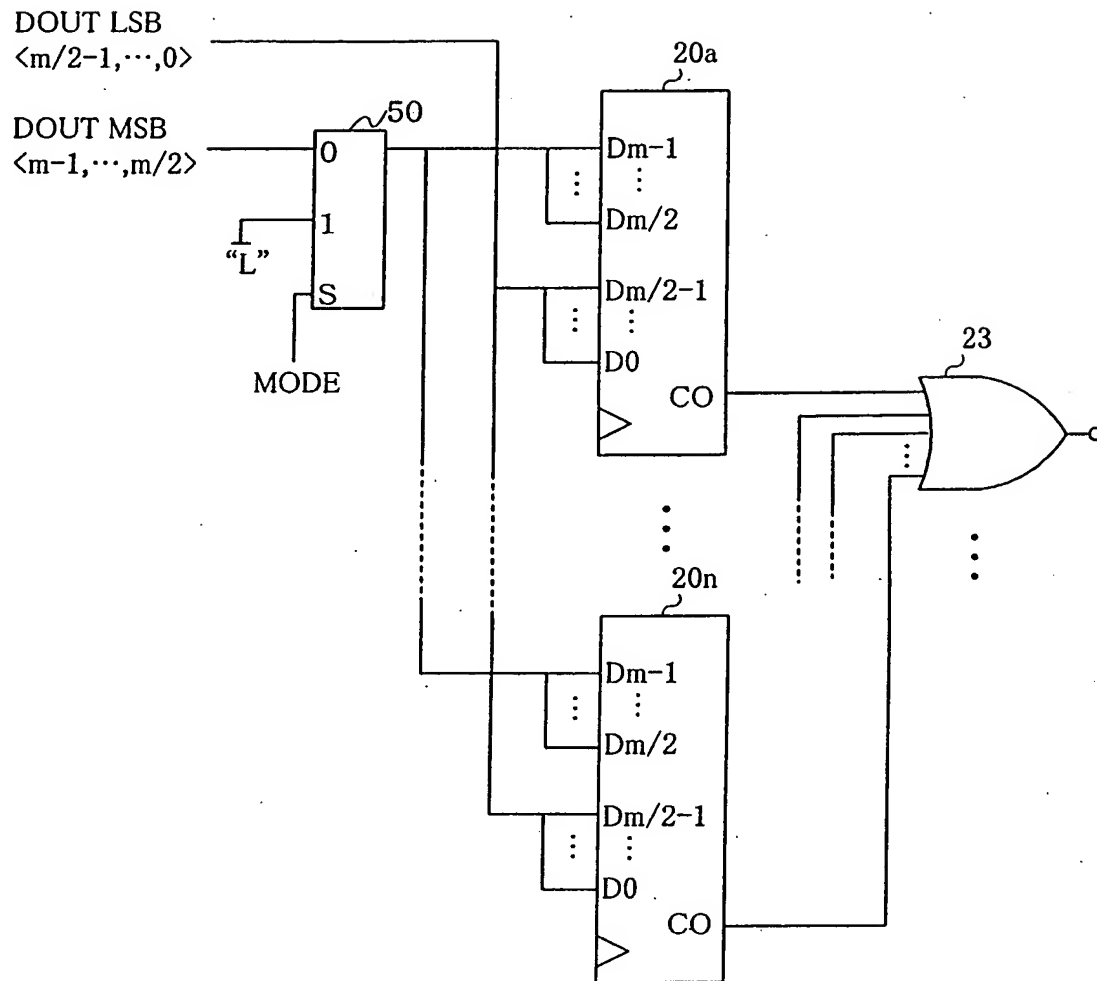
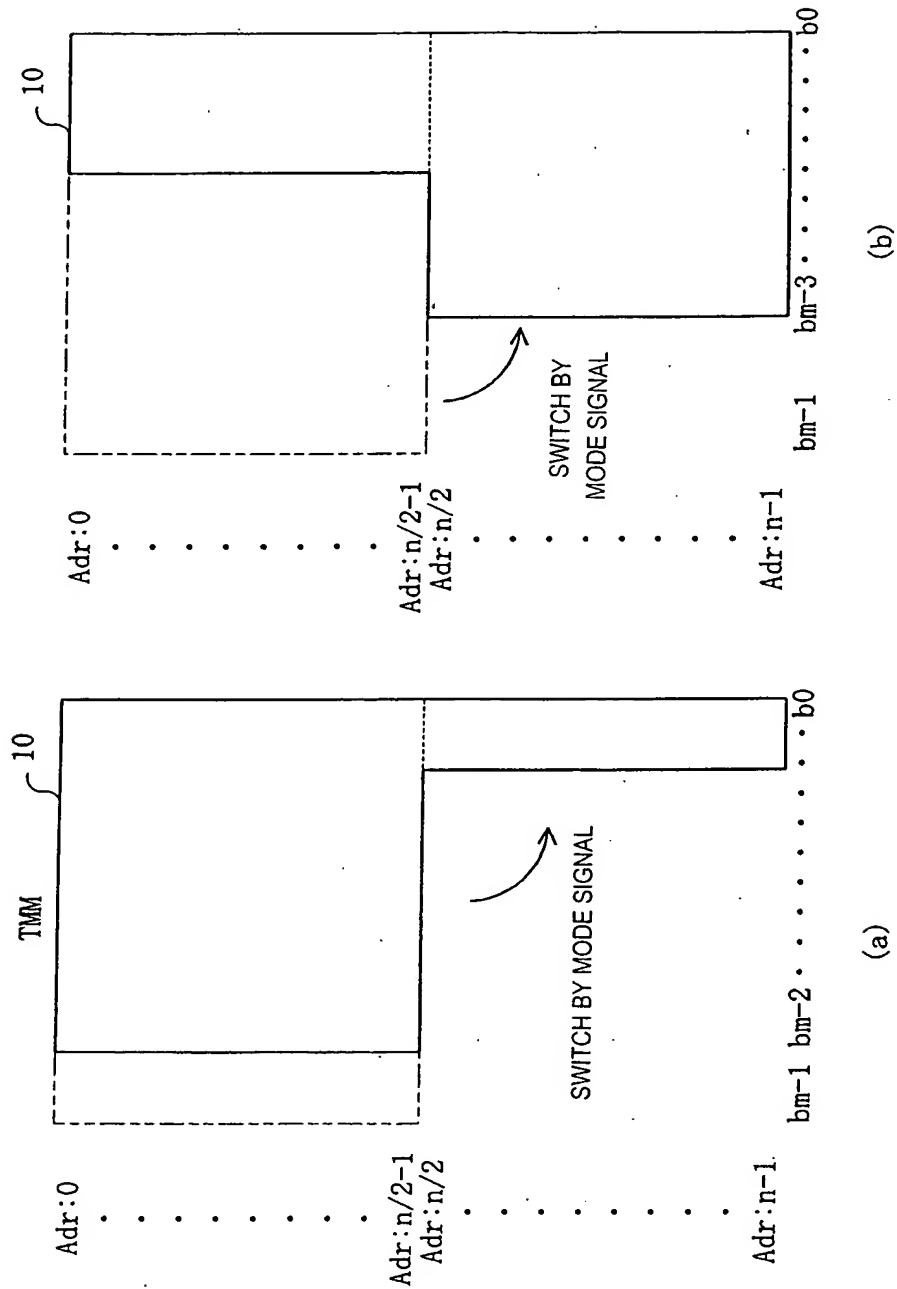


FIG. 8





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FIG. 9

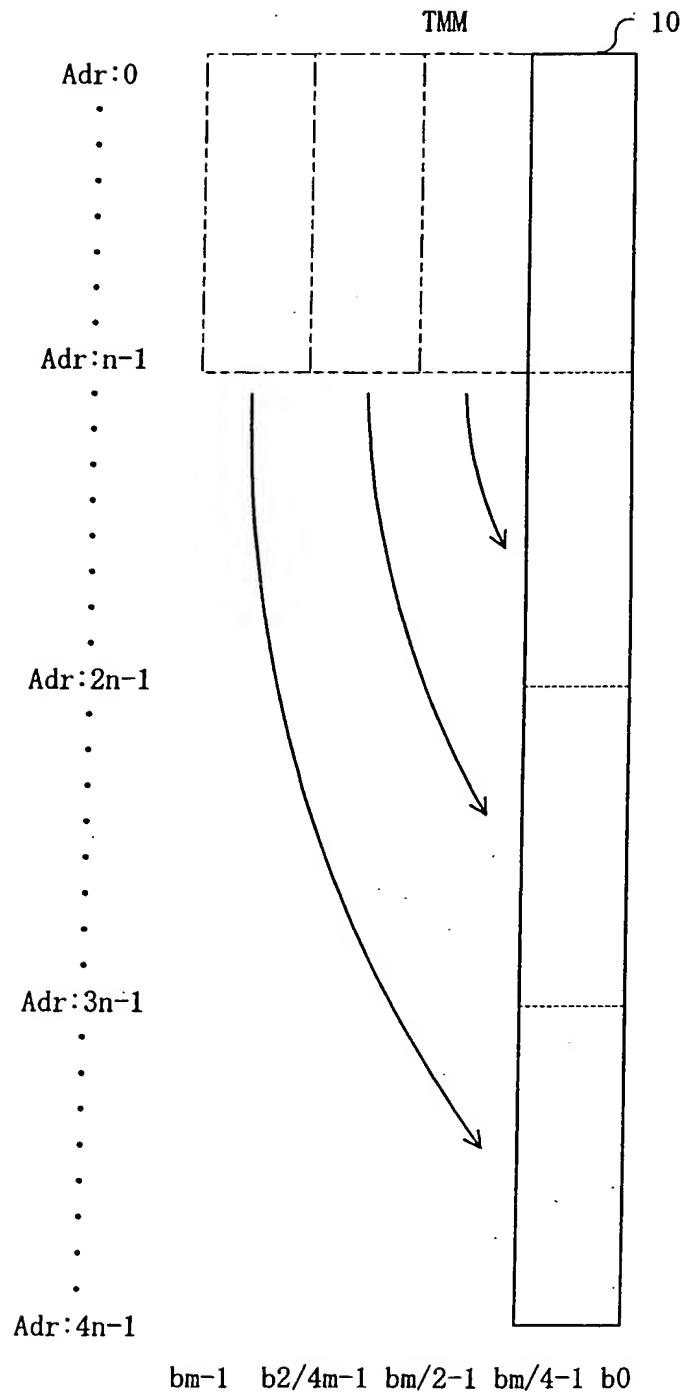


FIG. 10

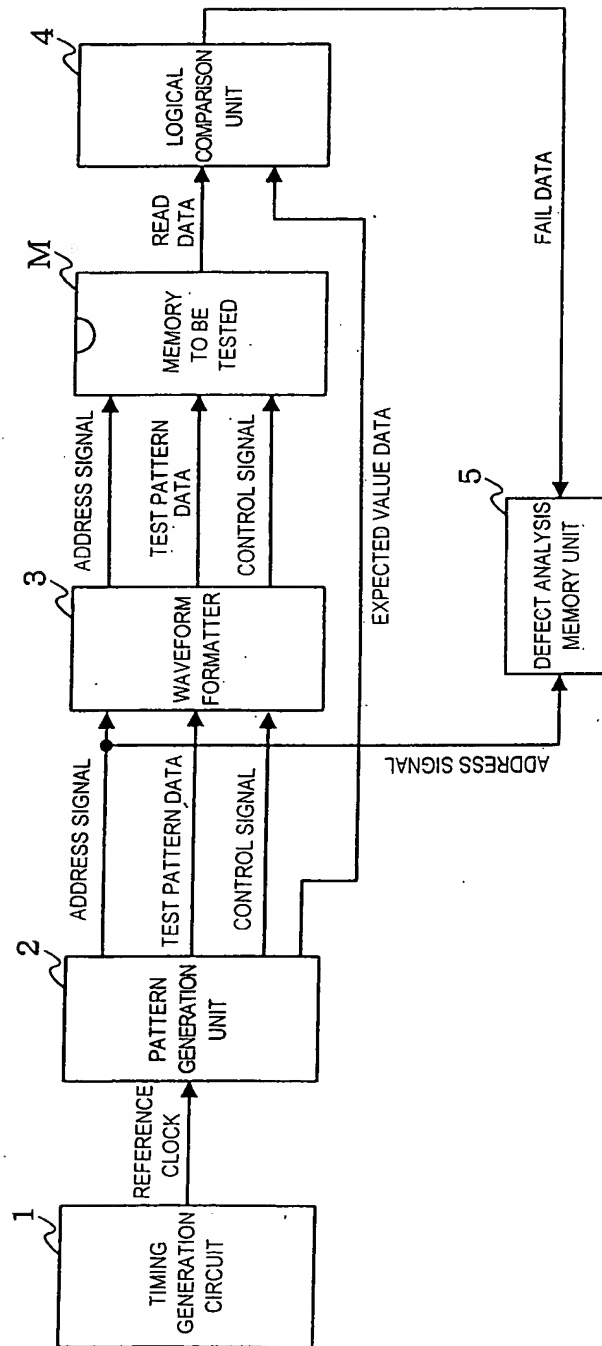
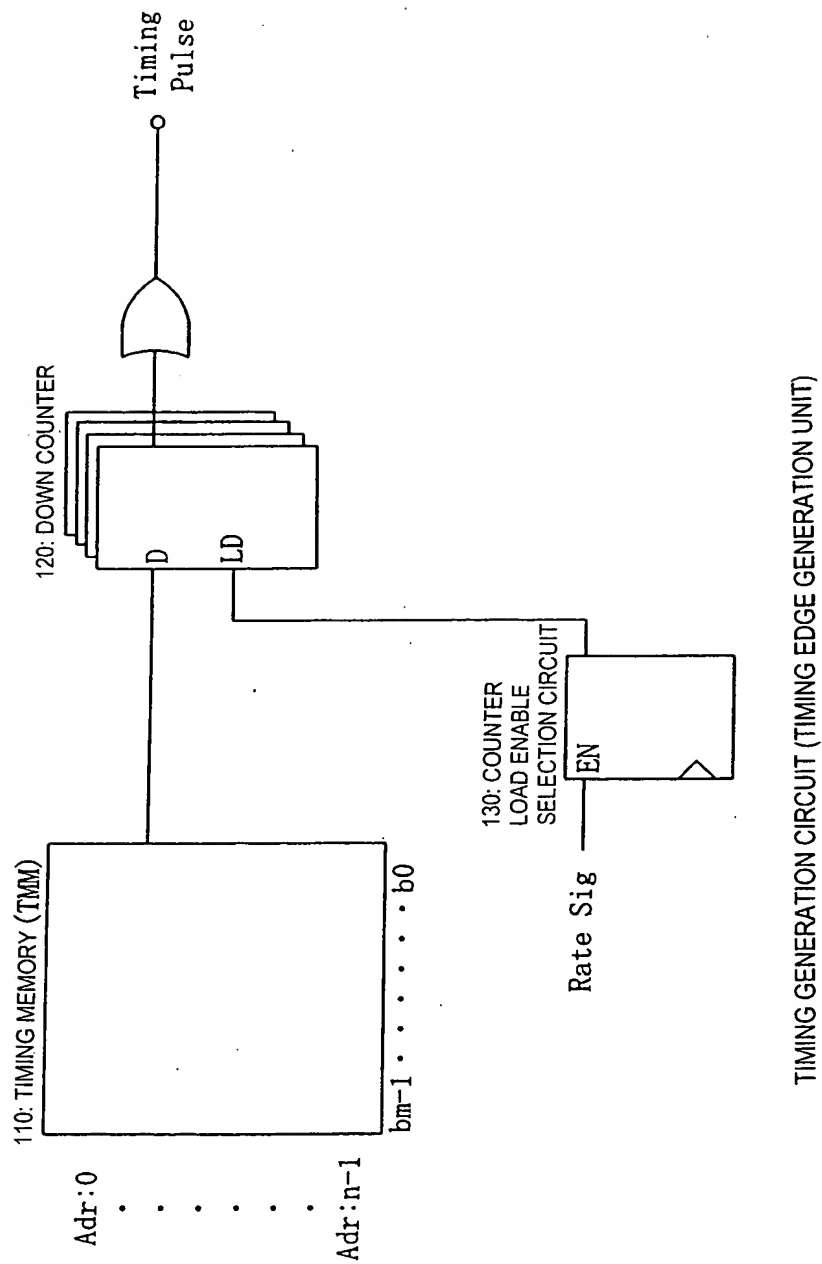


FIG. 11



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FIG. 12

